IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): John M. Cohn, et al.

Examiner: John P. Trimmings

Serial No: 10/709,754

Art Unit: 2117

Filed: May 26, 2004

Docket: BUR920040001US1 (17382)

For: A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA

Dated: November 16, 2007

Confirmation No: 3753

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT

Sir:

In response to the Office Action dated August 15, 2007, applicants respectfully request the Examiner to reconsider the application in view of the following amendments and remarks.

Amendments to the Specification begins on page 2 of this paper.

Amendments to the Drawings begins on page 3 of this paper.

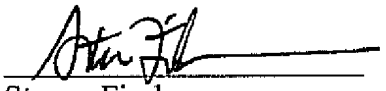
Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 11 of this paper.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on the date shown below.

Dated: November 16, 2007



Steven Fischman